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Code No: B5503

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(EMBEDDED SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1.a) Draw a neat block diagram of xilinx 3000 series I/O Block.
b) Briefly state the difference between CPLDs having sum of products architecture and look-up-table architecture.

2.a) How many dedicated product terms are available in a MAX 7000 S macro cell? How can this number of product terms be supplemented? What is the maximum number of product terms available to a macro cell?
b) State the possible clock configurations of a MAX 7000 S macro cell.

3. Implement a 2-bit binary counter using one 3000 series logic cell. The counter has an asynchronous reset (AR) and synchronous load (Ld). The counter operates as follows:
En = 0 No change
En = 1 Ld = 1 Load two flip flops with external inputs on rising edge of clock.
En = 1 Ld = 0 Increment counter on rising edge of clock.

4.a) Implement the 8-to-1 MUX using FLEX 10000 device. How many logic elerts are required?
b) Write a brief note on Optimized Reconfigurable Cell Array.

5. For the given ASM chart, draw a timing chart that shows the clock, the states (S0, S1 and S2) and input (x_1 x_2 x_3) and outputs. The input sequence is X_1 X_2 X_3 = 011, 101, 111, 010, 110, 101, 001. All state changes occur on the rising edge of the clock, and inputs change between clock pulses.
Derive next state and output equations by tracking link paths.

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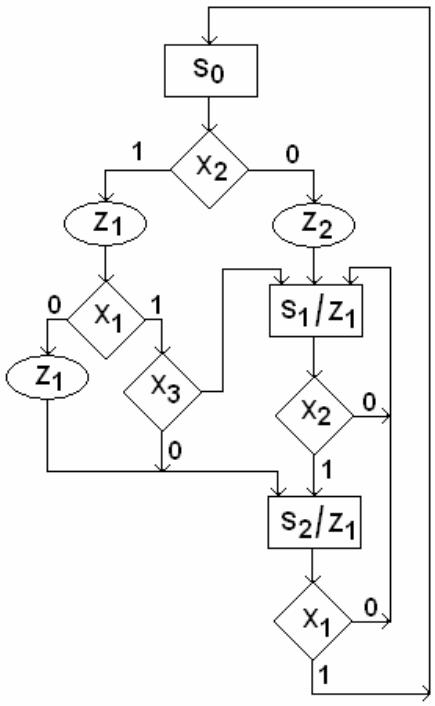

6.a) Compare the ACTEL'S ACT 1, 2, 3 in terms of their speed performance.

b) Draw a block diagram for a floating point subtractor. The fractions are 8 bits including sign, and the exponents are 5 bits including sign.

7. Design a 4 bit parallel adder using "FPGA advantage" tool.

8. Write brief note on:

a) Microprogramming linked state machines realization

b) CPLD vs FPGAs.

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